REMARKS

The Examiner rejected Claims 1-6 under 35 U.S.C. 103(a) as being unpatentable over Kumar *et al* (hereafter "Kumar")(US 2003/007 6899) in view of Kodama *et al.*(hereafter "Kodama") (US 7,023,324) Applicant traverses the rejection.

With respect to Claim 1, the Examiner states that Kumar teaches all the limitations of the Claim except for a multiplexer that outputs the filtered polyphase components in a predetermined order to generate a filtered output signal. The Examiner looks to Kodama for the missing teachings. Applicant disagrees with the Examiner's reading of Kumar as providing the Claim limitations apart from that relating to the multiplexer.

Claim 1 requires a plurality of filters, each filter processing a plurality of the polyphase components stored in the memory. The Examiner identifies elements 42a - 42m of Figure 1 as the plurality of filters required. Applicant submits that Figure 1 and the corresponding text on page 5 [0043] to page 6 [0045] show that each of the elements 42a - 42m acts only on the digital output of one of the corresponding analog to digital converters 32a – 32m, that each of these converters receives its input from one of the corresponding samplers 34a – 34m, and that each sampler receives the inphase and quadrature components of only one signal channel from the mixer 26. Hence, Applicant submits that each of the filters identified by the Examiner processes a single polyphase component, and not a plurality of polyphase components as required by the Claim. Kodama does not provide the missing teachings.

In addition, the memory identified by the Examiner stores the output of the analog-to-digital converters, not the polyphase components. The polyphase components are generated by the filters shown at 42a-42m. The buffers are at the output of the analog-to-digital converters, i.e., before the input to the filters.

Kodama teaches s multiplexer that operates on the polyphase components in place of the upsamplers shown in Figure 13a to generate a filtered polyphase signal. The Examiner has not indicated where the Examiner would place this multiplexer. If the multiplexer was

placed at the output of the polyphase filters shown at 42a-42m, it would serve no purpose. In the arrangement taught in Kumar, the FFT generator receives the outputs in parallel. If one were to use a multiplexer to load the filter outputs in the FFT, the system would lose the speed advantage obtained by the parallel processing.

Hence, Applicant submits that the Examiner has not made a *prima facie* case for obviousness with respect to Claim 1 and the Claims dependent therefrom.

With respect to Claim 2, the Examiner maintains that Kumar teaches that each filter utilizes the same functional relationship to generate the filtered polyphase components. The Examiner looks to paragraph [0033] as supporting this assertion. The paragraph in question refers to prior art devices, not the device taught in Kumar. Actually, Kumar teaches that the different filters have different coefficients (See paragraph [0055]). Hence, there are additional grounds for allowing Claim 2.

With respect to Claim 3, the Examiner maintains that Kumar teaches a buffer which the Examiner identifies as the memory recited in Claim 1. The Examiner maintains that it would be obvious to implement a shift register for this memory. The Examiner points to paragraph [0048] as supporting this assertion. Applicant must disagree with the Examiner's reading of the cited passage. The buffer referred to by the Examiner is part of the analog-to-digital converters. This buffer holds the output of the analog-to-digital converter prior to the output being shifted into the corresponding polyphase filter. The memory recited in Claim 1 stores the polyphase components for at least one cycle prior to the current polyphase cycle. The polyphase components are generated by the filters shown at 42a-42m in Kumar. The buffer in question does not store those outputs. Hence, even if one were to implement those buffers as shift registers, the limitations of the Claim 3 would not be met. In addition, Kumar teaches that the buffers are readout by a multiplexer, and hence, there is no reason to use a shift register. Hence, there are additional grounds for allowing Claim 3.

With respect to Claim 5, the Examiner maintains that Kumar teaches that the filters generate a filtered polyphase component that depends on a non-linear combination of the polyphase components. The Examiner points to paragraph [0033] as supporting this assertion. Applicant must disagree with the Examiner's reading of Kumar. First, the cited

paragraph discusses a prior art system, not the invention of Kumar. Second, Applicant can find no mention of any non-linear transformation in the cited paragraph or anywhere else in Kumar. Third, the system taught in Kumar performs a Fourier transform on the polyphase components. A Fourier transform is well known to be a linear transformation. Accordingly, Applicant submits that there are additional grounds for allowing Claim 5.

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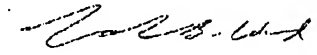
Respectfully Submitted,



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